

669270-26260

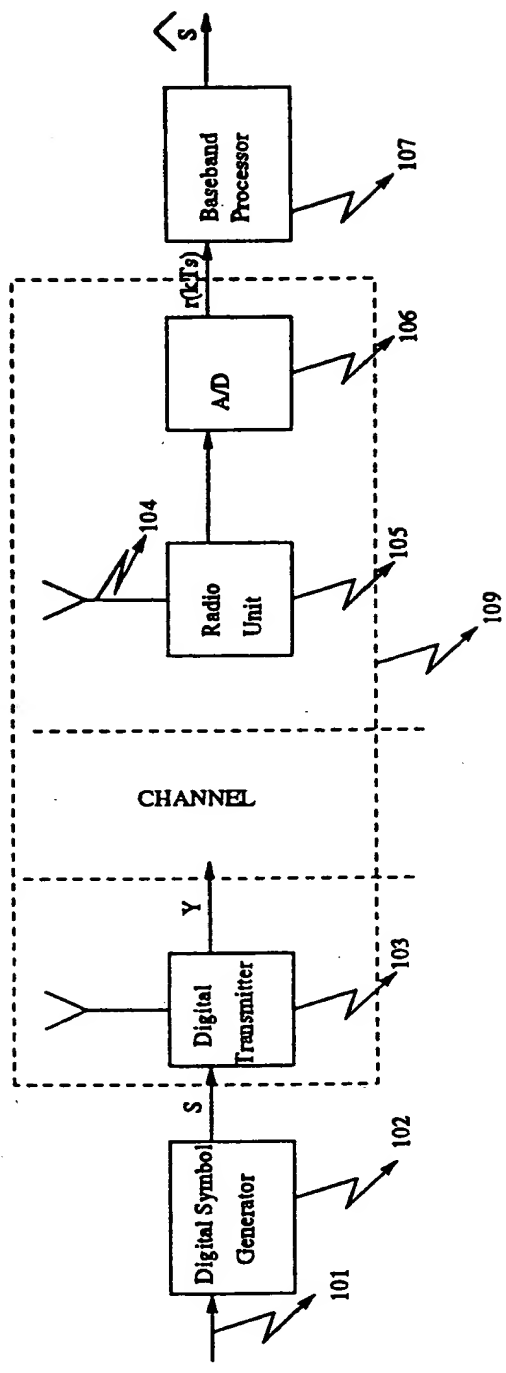


Figure 1

659470 947000

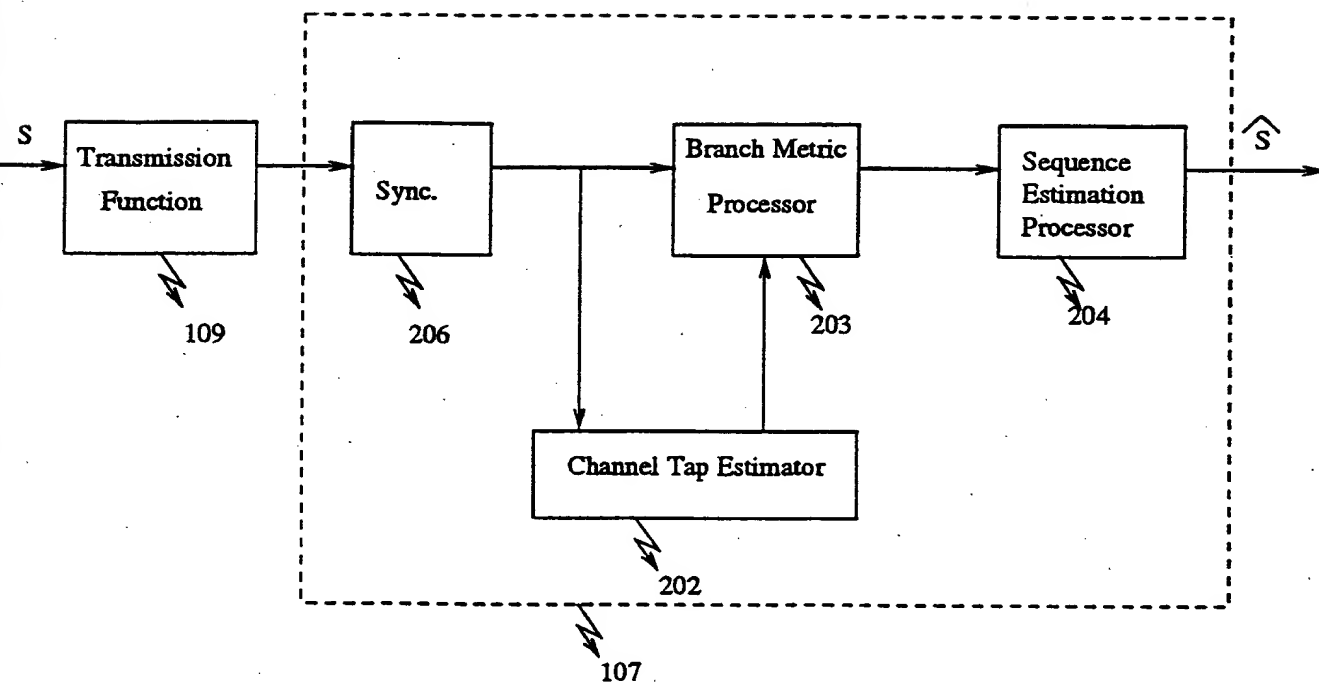


Figure 2

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graph LR
    S((S)) --> DT[Digital Transmitter]
    DT -- Y --> RC[Radio Channel]
    RC --> SUM((+))
    N((n)) --> SUM
    SUM --> RU[Radio Unit]
    RU --> AD[A/D]
    AD -- "r(kTs)" --> OUT(( ))
    
```

Figure 3

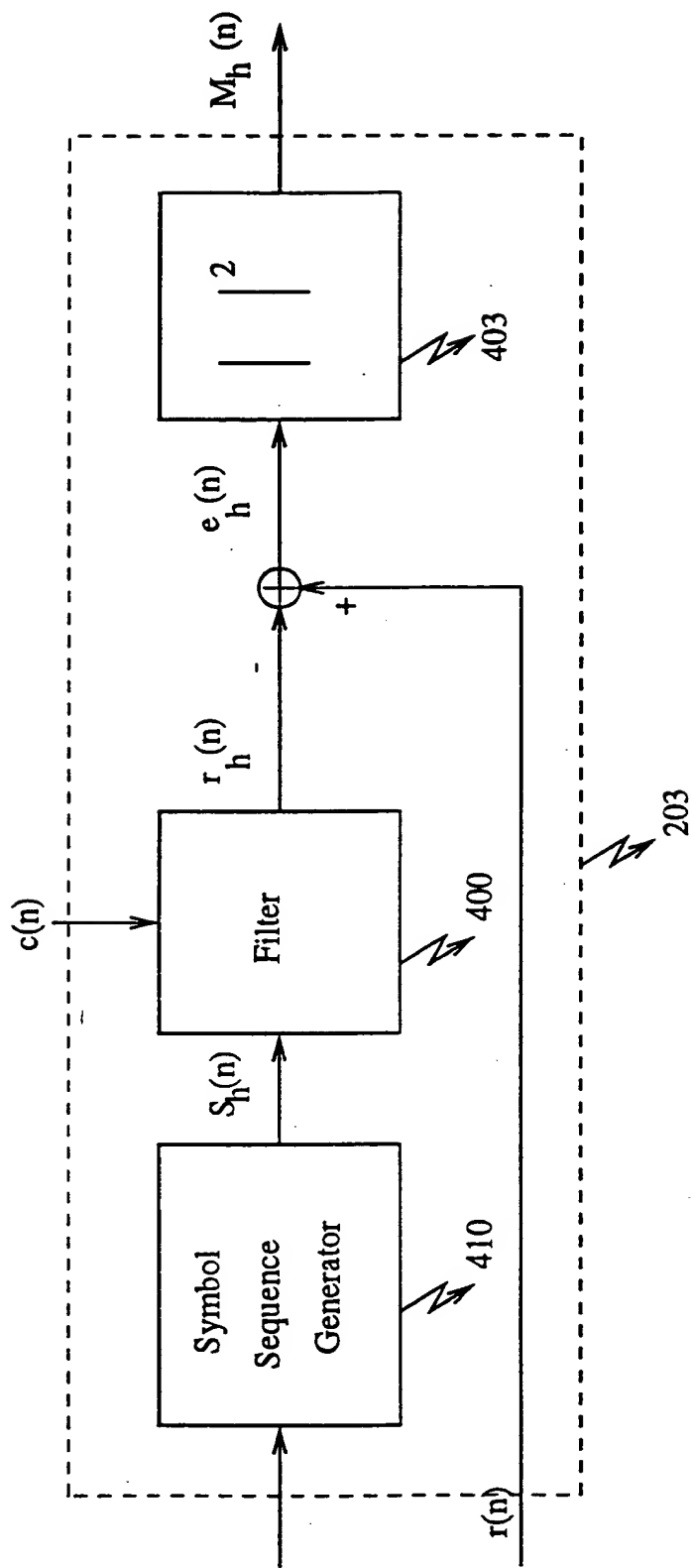


Figure 4

Figure 5 (PRIOR ART)

S_h \ $c(n)$	$c(0)B(1)$	$c(1)B(1)$	\bullet	\bullet	\bullet	$c(Nt-1)B(1)$
	$c(0)B(2)$	$c(1)B(2)$	\bullet	\bullet	\bullet	$c(Nt-1)B(2)$
				\bullet		
				\bullet		
				\bullet		
	$c(0)B(M)$	$c(1)B(M)$	\bullet	\bullet	\bullet	$c(Nt-1)B(M)$

500

Figure 6

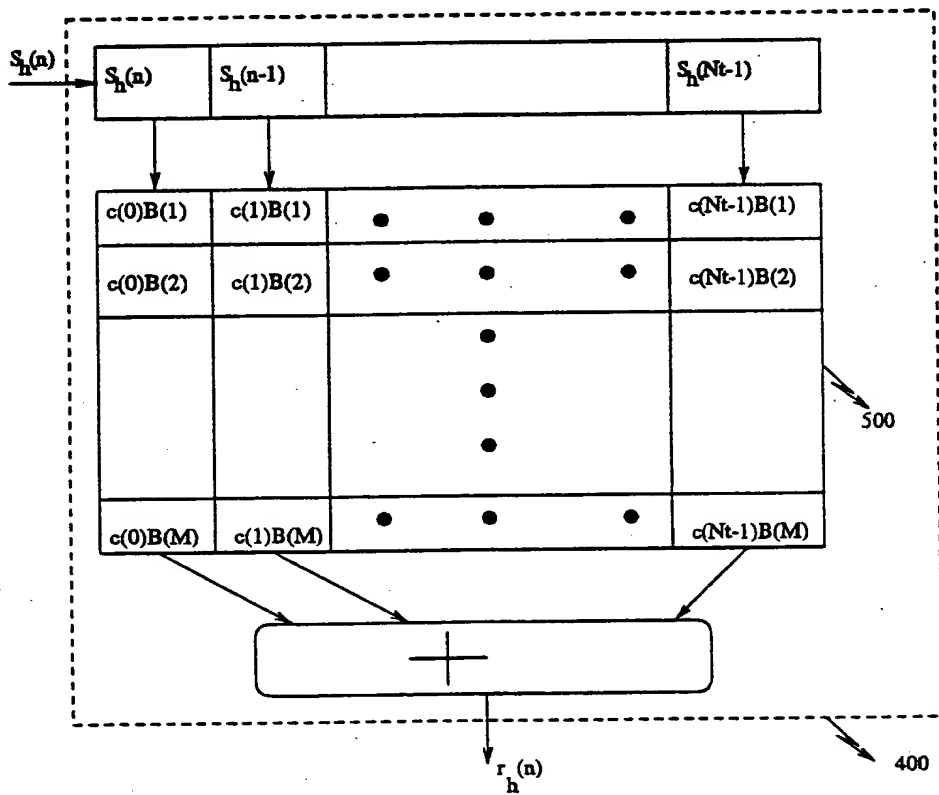


Figure 7

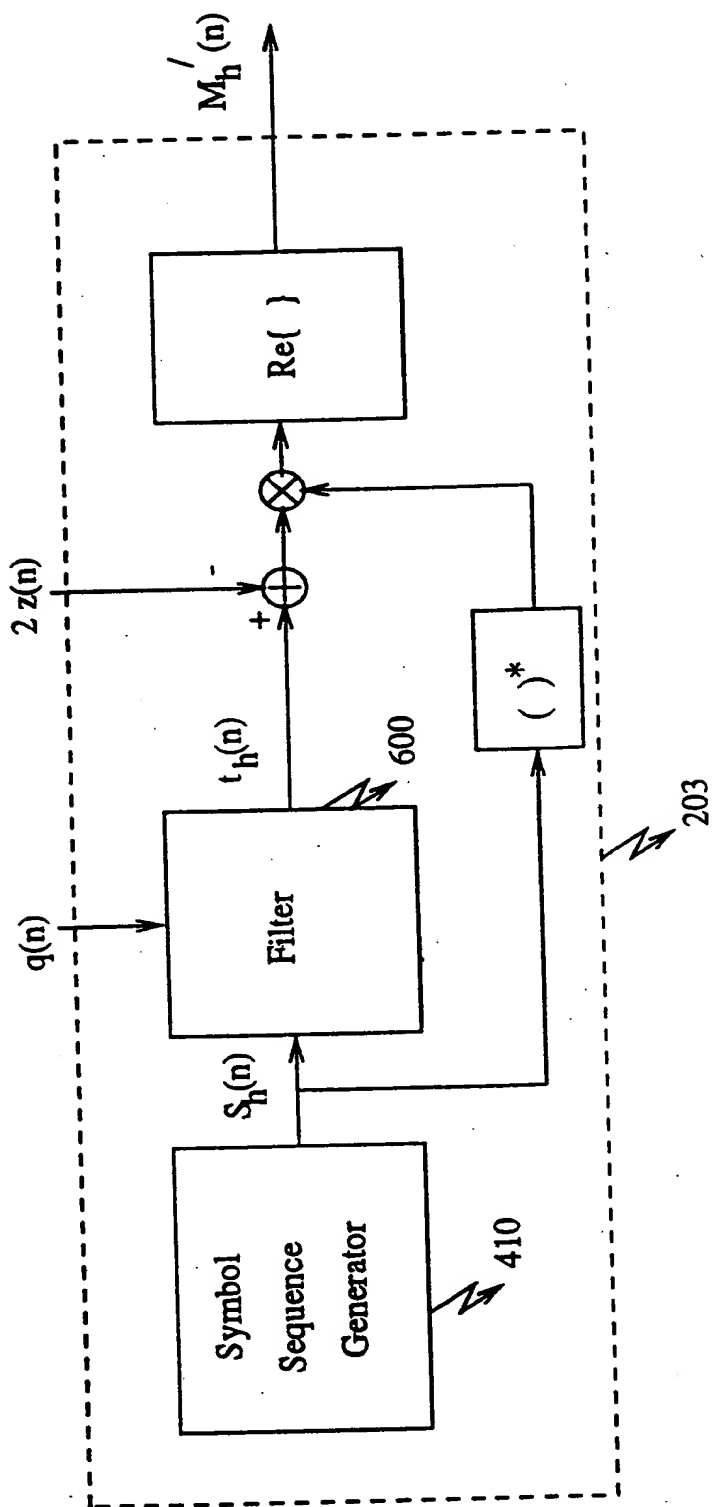


Figure 8

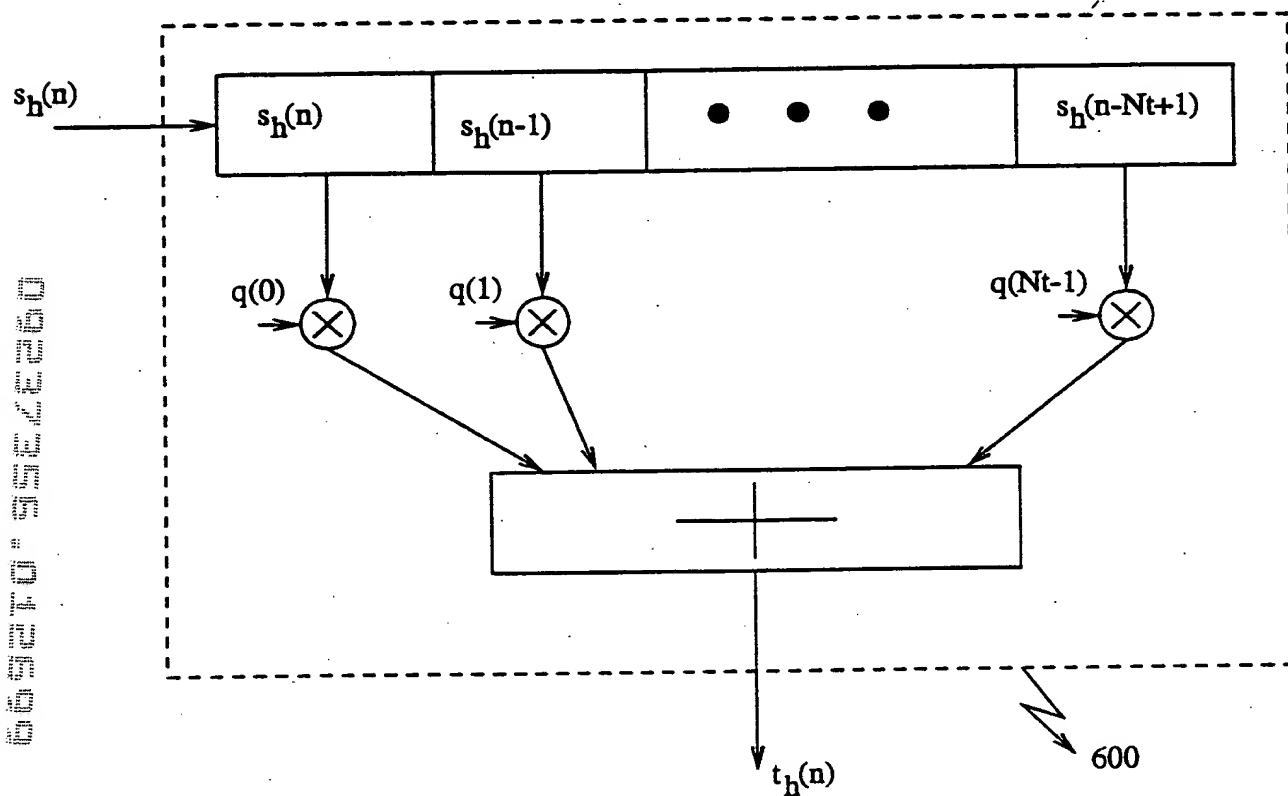


Figure 9. (PRIOR ART)

S_h

$c(n)$

$q(0)B(1)$	$q(1)B(1)$	• • •	$q(Nt-1)B(1)$
$q(0)B(2)$	$q(1)B(2)$	• • •	$q(Nt-1)B(2)$
		• • •	
$q(0)B(M)$	$q(1)B(M)$	• • •	$q(Nt-1)B(M)$

\swarrow
550

Figure 10

The diagram illustrates a parallel FIR filter structure. The input signal $s_h(n)$ is fed into a register that stores $s_h(n)$, $s_h(n-1)$, and $s_h(Nt-1)$. These signals are then fed into a parallel structure of M filter branches. Each branch contains a delay element z^{-1} and a multiplier. The outputs of the branches are summed to produce the final output $t_h(n)$.

Figure 11